Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CLEAR**
2. **CLOCK**
3. **A**
4. **B**
5. **C**
6. **D**
7. **ENABLE P**
8. **GND**
9. **LOAD**
10. **ENABLE T**
11. **QD**
12. **QC**
13. **QB**
14. **QA**
15. **RIPPLE CARRY**
16. **VCC**

**.083”**

**.109”**

**15**

**16**

**1**

**2**

**3**

**14 13 12 11**

**4 5 6 7**

**10**

**9**

**8**

**MASK**

**REF**

1021**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential:**

**Mask Ref: 10215**

**APPROVED BY: DK DIE SIZE .083” X .109” DATE: 10/20/21**

**MFG: RCA THICKNESS .020” P/N: CD40161B**

**DG 10.1.2**

#### Rev B, 7/1